

**In the Claims:**

1. (Currently Amended) A semiconductor integrated circuit, the circuit comprising:  
a silicon substrate having a substantially planar top substrate surface;  
a silicon epitaxial layer having that has a lower resistivity than the resistivity of said silicon substrate, the epitaxial layer having a substantially planar lower epitaxial surface, the epitaxial layer being formed upon the top substrate surface so that the lower epitaxial surface and the top substrate surface are adjacent;  
~~first and second circuit sections~~ a first and a second circuit section formed in said silicon epitaxial layer, each circuit section spaced apart from the top substrate surface by a respective portion of the silicon epitaxial layer; and  
a device isolation region ~~projecting from said silicon substrate up to a surface of each of said first and second circuit sections~~ formed toward an inner part of the epitaxial layer from the top surface of the epitaxial layer between said first and second circuit sections sections;  
\_\_\_\_\_ wherein the portions of the epitaxial layer under both the first and second circuits are in contact with the substrate.
2. (Previously Presented) The semiconductor integrated circuit according to Claim 1, wherein the resistivity of said silicon substrate is between 20 and 100 times the resistivity of said silicon epitaxial layer.
3. (Previously Presented) The semiconductor integrated circuit according to Claim 2, wherein the resistivity of said silicon substrate is between 50 and 100 times the resistivity of said silicon epitaxial layer.
4. (Canceled).
5. (Currently Amended) The semiconductor integrated circuit according to Claim 1, wherein a digital circuit is formed on said ~~first~~ first circuit section, and an analog circuit is formed on said second circuit section.

6-10. (Cancelled)

11. (Previously Presented) The semiconductor integrated circuit according to Claim 1, wherein said silicon epitaxial layer is a single layer.

12. (Previously Presented) The semiconductor integrated circuit according to Claim 1, wherein said silicon epitaxial layer is a p-type bulk epitaxial layer.

13. (Previously Presented) The semiconductor integrated circuit according to Claim 12, wherein said silicon substrate comprises a p-type bulk substrate.

14. (Previously Presented) The semiconductor integrated circuit according to Claim 13, wherein a first impurity concentration of the p-type bulk substrate is one-hundredth or less a second impurity concentration of the p-type bulk epitaxial layer.

15. (Previously Presented) The semiconductor integrated circuit according to Claim 13, wherein said silicon substrate has a thickness of 0.7mm and a resistivity of 1000 Ohm – cm.

16. (Previously Presented) The semiconductor integrated circuit according to Claim 12, wherein said p-type bulk epitaxial layer is formed by a chemical vapor deposition method.

17. (Previously Presented) The semiconductor integrated circuit according to Claim 12, wherein said silicon epitaxial layer has a thickness of 5 micrometers and a resistivity of 10 Ohm – cm.

18. (previously presented) The semiconductor integrated circuit according to Claim 1, wherein said silicon substrate and said silicon epitaxial layer are of the same conductivity type.